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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

U.S. Patent No.	: 6,797,997	Confirmation No.:	2246
First Named Inventor	: Yoji HATA		
Issued	: September 28, 2004		
Examiner	: H.B. Trinh		
Docket No.	: 037133.52558US		
Customer No.	: 23911		
Title	: Semiconductor Memory Apparatus		

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322(a)

Attention: Certificates of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is respectfully requested that the attached Certificate of Correction be entered in the patent identified above. Claims 1 and 2 contain mistakes of a typographical nature and of minor character. These mistakes do not constitute new matter or require reexamination. Accordingly, please correct claims 1 and 2 as noted on the attached Certificate of Correction.

The fee of $100 as set forth in 37 C.F.R. § 1.20(a) is enclosed. Please charge any additional fees to the undersigned counsel's Deposit Account 05-1323, Docket No. 037133.52558US.

10/24/2005 HLE333 00000071 051323 6797997
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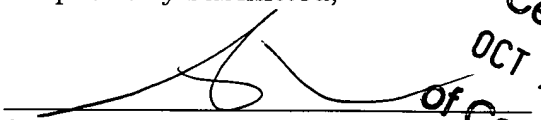
October 21, 2005

Respectfully submitted,



Certificate OCT 26 2005 of Correction

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,797,997 B2

DATED : September 28, 2004

INVENTOR(S) : Yoji HATA et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please change claim 1 in col. 7, lines 30-47 as follows:

1. A method for storing data by accumulating charges in a capacitor, comprising:

~~before performing a precharge for bringing the potential of a pair of bit lines to an intermediate potential by making a short circuit in the pair of bit lines, the potential of the bit line being charged to a higher level is previously lowered to a level within the range that prevents data written in a memory cell from being disappeared~~

lowering a potential of a first bit line of a pair of bit lines to a level within a range that prevents data in a memory cell from being lost; and

making a short circuit between said pair of bit lines to perform a precharge of said pair of bit lines by bringing the potential of said pair of bit lines to an intermediate potential,

wherein said short circuit is made after said lowering occurs.

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PATENT NO. 6,797,997

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,797,997 B2

DATED : September 28, 2004

INVENTOR(S) : Yoji HATA et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Please change claim 2 in col. 7, lines 48-67 to col. 8, lines 1-3 as follows:

2. A semiconductor memory apparatus for storing data by accumulating charges in a capacitor, comprising:

a forced step-down circuit ~~comprised of~~ comprising a first switching element having one end connected to a driving line on the high side, ~~and~~

a forced step-down capacitor and a second switching element arranged in parallel between the other end of the first switching element and a ground potential, and

a pair of bit lines, wherein a first bit line of said pair of bit lines is connected to said driving line, wherein

the second switching element is brought into an on state ~~in advance~~ to hold the forced step-down capacitor at zero potential before the first switching element is brought into an on state, and

before making a short circuit in the pair of bit lines to perform ~~performing~~ a precharge ~~for~~ by bringing a potential of a pair of bit lines to an intermediate potential ~~by making a short circuit in the pair of bit lines~~, the first switching element is ~~then~~ brought into an on state to lower ~~and~~ a potential of the driving line on the high side ~~is previously lowered~~ to a level within ~~the~~ a range that prevents ~~of preventing~~ data written in a memory cell from being lost ~~disappeared~~.

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